FORM PTO-1390 (REV 11-2000)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 36-1534
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 09/980460 Unknown
INTERNATIONAL APPLICATION NO. PCT/GB00/02531	INTERNATIONAL FILING DATE 30 June 2000	PRIORITY DATE CLAIMED 1 July 1999

TITLE OF INVENTION

DATA PROCESSING APPARATUS

APPLICANT(S) FOR DO/EO/US

MACKICHAN et al

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items or information.

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/980460 Unknown	PCT/GB00/02531	36-1534

21. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):		
-- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00		
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00		
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO $740.00		
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00		
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$ 0.00	

CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE			
Total Claims	11	-20 =	0	X	$18.00	$ 0.00	
Independent Claims	2	-3 =	0	X	$84.00	0.00	
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)					$280.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =						$ **890.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.						0.00	
SUBTOTAL =						$ **890.00**	
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +						0.00	
TOTAL NATIONAL FEE =						$ **890.00**	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property +						$ 40.00	
Fee for Petition to Revive Unintentionally Abandoned Application ($1280.00 – Small Entity = $640.00)						$ 0.00	
TOTAL FEES ENCLOSED =						$ **930.00**	
						Amount to be: refunded	$
						Charged	$

a. ☒ A check in the amount of $930.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.
d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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25,640 REGISTRATION NUMBER

December 4, 2001 Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

MACKICHAN et al

Atty. Ref.: **36-1534**

Serial No. **Unknown**

Group:

National Phase of: **PCT/GB00/02531**
International Filing Date: **30 June 2000**

Filed: **December 4, 2001**

Examiner:

For: **DATA PROCESSING APPARATUS**

* * * * * * * * * * *

December 4, 2001

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

Prior to calculation of the filing fee and in order to place the above identified application in better condition for examination, please amend as follows:

IN THE SPECIFICATION

Page 1, after the title insert the following:

-- This application is the US national phase of international application PCT/GB00/02531 filed June 30, 2000 which designated the U.S. --.

IN THE CLAIMS

Please substitute the following amended claims for corresponding claims previously presented. A copy of the amended claims showing current revisions is attached.

3. (Amended) Apparatus according to claim 1 wherein at least one of the processors is operable to carry out processing according to a plurality of different algorithms and to select at least one of them according to the outcome of processing performed by another of the processors.

4. (Amended) Apparatus according to claim 1 wherein the backplane includes a first conduit for signals in a first format and a second conduit for signals in a second format.

6. (Amended) Apparatus according to claim 4 wherein the processors include a first processor to process signals derived from the first conduit and a second processor to process signals derived from the second conduit.

7. (Amended) Apparatus according to claim 4 including an input to receive input signals to be processed and to supply the signals to the first and second conduits in the first and second formats.

8. (Amended) Apparatus according to claim 4 wherein the first and second conduits are configured to convey optical and electrical signals respectively.

11. (Amended) A method according to claim 9 including selecting the processing for data in one of the formats from a plurality of different algorithms according to the outcome of processing performed on the data in another of the formats.

REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The above amendments are made to place the claims in a more traditional format.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

3. (Amended) Apparatus according to claim 1 [or 2] wherein at least one of the processors is operable to carry out processing according to a plurality of different algorithms and to select at least one of them according to the outcome of processing performed by another of the processors.

4. (Amended) Apparatus according to [any preceding claim] claim 1 wherein the backplane includes [an] a first conduit for signals in a first format and a second conduit for signals in a second format.

6. (Amended) Apparatus according to claim 4 [or 5] wherein the processors include a first processor to process signals derived from the first conduit and a second processor to process signals derived from the second conduit.

7. (Amended) Apparatus according to claim 4[, 5 or 6] including an input to receive input signals to be processed and to supply the signals to the first and second conduits in the first and second formats.

8. (Amended) Apparatus according to [any one of claims 4 to 7] claim 4 wherein the first and second conduits are configured to convey optical and electrical signals respectively.

11. (Amended) A method according to claim 9 [or 10] including selecting the processing for data in one of the formats from a plurality of different algorithms according to the outcome of processing performed on the data in another of the formats.

Data Processing Apparatus

Field of the invention

This invention relates to a data processing apparatus.

Background

Traditional computer architectures systems are well suited to processing data according to predefined algorithms such as by a conventional Von Neumann digital processor. However, such conventional data processing is not generally suited to problems involving analog signals, pattern matching and asynchronous or real-time signals, and also in noisy or chaotic systems or those where the algorithm to be used is unknown and is to be determined by processing of the data.

Neural nets have been proposed for pattern recognition and other purposes but they are not able to adapt rapidly to changes in the system parameters and require extensive training.

The present invention seeks to provide an improved general purpose data processing apparatus which overcomes these difficulties.

Summary of the invention

According to the present invention there is provided data processing apparatus comprising: a backplane for data signals in a plurality of different formats, a plurality of adaptive filters to receive data signals in respective different formats from the backplane, a plurality of processors to receive data derived from the backplane in said different formats respectively, at least one of the processors being operable to process data from one of the filters and being responsive to the outcome of data filtering performed by at least one other of the filters to adapt the processing performed thereby.

The apparatus according to the invention is not limited to any particular technology, medium or transport mechanism for the signals of different formats, which for example, can be optical, electrical, chemical or any other suitable form.

The use of signals in different formats allows data to be analysed from different perspectives so that a processor operable with signals in a first format may be configured to perform efficient processing on the basis of an analysis of the signals in a second different format.

To this end, a feedback path may be provided to adjust filtering characteristics of at least one of the adaptive filters as a function of the outcome of the processing performed by at least one of the processors.

The feedback may be configured to achieve homeostasis.

At least one of the processors may be operable to carry out processing according to a plurality of different algorithmic processes and to select one of them according to the outcome of the processing performed by another of the processors. Thus, the processing of data in one of the formats can be used to optimise processing of the data in another of the formats so as to provide more efficient algorithmic processing of the data.

Brief description of the drawings

In order that the invention may be more fully understood an embodiment of thereof will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a schematic block diagram of an architecture for a data processing apparatus according to the invention;

Figure 2 is a schematic diagram of operation of the architecture shown in Figure 1;

Figure 3 is a schematic illustration of the relationship between an entity and its attributes;

Figure 4 is a schematic diagram of how entities are related through their attributes; and

Figure 5 is a schematic block diagram of a code breaking machine in accordance with the invention.

Detailed description

Referring to Figure 1, the data processing apparatus includes an array of sensors 1 which provide signals in a number of different formats relating to an external environment in response to inputs I. The sensors 1 produce outputs in different signal formats which are fed into a multi-format communications backplane 2. As explained in more detail hereinafter, the backplane 2 acts as a conduit for signals in different formats, such as optical, electrical, chemical.

A series of connections 3 extend from the backplane 2, to individual adaptive filters 4 which individually recognise some physical property of signals on the backplane 2. For example, one of the filters 4 may be an optical filter configured to recognise a particular optical characteristic of signals from the backplane whereas another one of the filters 4 may be an electrical filter for filtering electrical signals from the backplane. The filters may recognise characteristics such as frequency or some other characteristics such as the signal's chaotic state.

Each of the adaptive filters 4 has an associated processor 5 capable of processing signals in the individual formats handled by the filters. The result of the filtering and processing is fed back on path 6 to the backplane 2 so that the processed signals can be then pass to another filter-processor combination 4, 5 for further processing.

As shown in Figure 1 processor 5a produces an output 6a which passes out of the apparatus. Additionally, an array of transducers/effectors 7 can be provided, responsive to the outputs of the processors 5 to provide an output 6 which can be used to control other processor/filter combinations or communicate with external apparatus.

In operation, inputs I are present in the environment, are detected by the sensor array 1 so as to place signals on the universal backplane 2. The signals may be of any suitable form in different formats, as previously described, and the role of the backplane 2 is to ensure that all of the processor/filter components can receive signals in corresponding appropriate formats from the backplane. The formats may

include optical, photonic, liquid or gaseous movement, changes of state and the connections may be achieved in free space or constrained for example in a fibre or tube. Modes of communication may be analog or digital in the backplane 2. Preferably, the modes of communication in the backplane are inherently multi-modal. For example, an optical fibre can transmit both on many wavelengths and either analog or digital signals. The backplane 2 may perform differential attenuation of signals and may exhibit different temporal characteristics to different signals.

The adaptive filters 4 connected to the backplane 2, select from the signals of different formats those that they can recognise. This will depend on the physical properties and the algorithmic nature of the signal. For example, an optical filter 4 can be set to a particular wavelength, signal threshold and window time, thus acting as a filter element tuned to particular signals. The filter can also act as a buffer by looking only for signals that exhibit a particular short term periodicity. The filter would respond purely to analog signals at the same wavelength and thus some signals from the backplane can strongly stimulate certain filters and weakly or differentially be detected by other ones of the filters.

The filters 4 are adaptive and thus change their filtering properties according to the signals that are acted upon by them. The filtered signals 6 are used to adjust the characteristics of the filters 4 adaptively.

The more that a processor 5 responds to a particular filtered signal, the stronger should be the reinforcement. The filter 4 can be considered as accepting signals inside certain bounds which the overall apparatus can alter. For example, bounding of the filtered signals in terms of wavelength, threshold and window duration can be carried out. The effect of the feedback to the adaptive filters 4 is either to increase or decrease bounding of the filter. The exact mechanism will depend on the processor 5 and the filter 4. The goal is to reinforce desirable behaviours. The bounding could even initially increase response strength and then decrease so that the filter 4 self-tunes to an optical response level.

The processors 5 are configured to receive filtered inputs from the filters 4 and to carry out an algorithmic process to provide an output. The processors 5 may take many different forms. They may comprise conventional digital processors or can operate according to an analog computation, involve interaction with humans, be a wet chemical, electronic or other action. The processors 5 may include individual memories to store precise, imprecise or temporally failing data. Unlike a conventional Von Neumann processor, there may not be a requirement for a dedicated conventional memory store, but instead, memory elements may be distributed throughout the processor architecture, for example in the backplane 2 or the filters 4.

Figure 2 provides an insight into how the architecture will operate to produce an effective output 6, having been stimulated at its input 1a.

In Figure 2, a number of vectors are shown, as follows:

P	Vector that represents a problem space
K	Vector that represents a knowledge space
S	Vector that represents a solution space
B	Vector that represents a bounding function
erf I	Vector that represents an error function

The apparatus in basic terms produces a solution, or a manipulation of an effector, by operating a transform from the problem space P which acts with the knowledge space K to create a solution or a number of solutions in the solution space S. The bounding vector B is used to bound the solution.

The error function erf I is used to stimulate the machine randomly and/or synchronously in order to prevent it from falsely locking into a limited solution space. Although in Figure 2, the process is presented in two dimensions for each of explanation, it will be understood that the architecture of Figure 1 has the capability to operate in N dimensions.

Each element of the P, K, and S vectors consist of a single entity which has a number of attributes associated with it, as indicated in Figure 3. The machine builds its knowledge space K by creating entities and associate attributes with each entity. The machine links the attributes, which are not permanent in time, and the links are continually reviewed and reinforced as appropriate. If the links are used often, then they are reinforced because it indicates a strong association between the entity and the attribute. If the link is used less often, it is weak and is removed relatively quickly.

Figure 4 illustrates schematically how entities are related through their attributes. Figure 4 illustrates entity groups E1, E2, E3, and E4 and E5.

Knowledge K is associated with an entity E, where:

E1 represents a dog
E2 represents a cat
E3 represents a mink
E4 represents a car
E5 represents a locomotive

An attribute that could link groups E1, E2 and E3 is fur. An attribute that could link group E4 and E5 is steel.

The same rules apply to the linking of attributes as to the linking of an entity to an attribute.

Example

The architecture shown in Figure 1 together with the functionality described with reference to Figures 2 and 3 can be used with advantage to provide a code breaker and an example of code breaker machine architecture is shown in Figure 5.

There is an inherent problem with employing conventional digital computers to crack encrypted code. The conventional method is to use a plurality of code cracking algorithms which are coded into the computer and then the computer

number crunches until it achieves a solution, if possible. A problem with this method is that there are a large number of data combinations that the computer needs to investigate and so if it starts in the right part of the checking sequence, it could reach a solution relatively quickly whereas if it starts spuriously in the wrong part of the solution space, the solution may take much longer to achieve.

In accordance with the invention, this inefficiency is improved by using additional processing techniques on the signals in different formats in order to provide the computer with an indication of where to start looking for a solution. This minimises the random nature of how long the digital computer takes to break code. Conventional code breaking algorithms are run on processor/filter combinations 4a/5a, and additional processing is carried out by processors and filters 4b, 5b and 4c, 5c.

An electrical signal I, which may comprise a signature or password created by the multiplication of two prime numbers, is fed as an input to the element 1, which produces signals in two different formats. In this example, the element 1 comprises an electro-optical modulator, e.g. a laser which receives the input signals I as electrical signals and converts them into corresponding optical pulses. The backplane 2 comprises an electrical line 2a e.g. a coaxial cable which acts as a conduit for the input digital electrical signals I. The modulator 1 produces corresponding digital optical signals that are fed to a second conduit 2b in the form of an optical fibre.

A processor 5b, in the form of a spectral analyser is responsive to the characteristics of the electrical signals in the backplane 2. The analyser 5b is capable of making measurements e.g. from 0-10 GHz with integral filtering functionality thereby providing an inherent adaptive filter 4b. When the element 5b initially senses the electrical coded signal I on the conduit 2a, its filter 4b is set to maximum bandwidth namely 0 - 10GHx. The analyser then takes measurements in relation to the signal frequency, amplitude and power of the signals and upon analysing the measurements, modifies the bandwidth of the filter in order to band limit the spectrum of measurement. This modification of the filter from its maximum bandwidth to a band limited value, constitutes learning and homeostasis, as the

filtering is adapted in response to an analysis of the incoming electrical signal. As long as there is no or little change in the input coded signal from conduit 2a, the filtering will stay in a relatively constant state, but will change in response to changes in the input signal characteristics. Additionally, data from the filter 4a/processor 5a can provide feedback through the electrical wiring to the filter 4b to allow its characteristics to be adaptively changed. Examples of suitable spectrum analysers are HP4395-500MHz, HP4936-1.8GHz, HP8757-40GHz.

The optical signals produced on the conduit 2b are detected by a processor/filter arrangement 5c, 4c capable of performing an optical Fourier transform. The device may comprise a dispersive optical element which has an array of optical receivers which form the output of the filter 4c. When the optical signal is presented to the Fourier transformer, it produces a corresponding pattern in the focal plane of the device which is detected and hence characterised by the optical receiver array 4c. When the coded signal applied to the transformer is modified, the output from the array is consequently changed. The element 4c/5c includes a memory and a simple processing capability to enable particular output patterns for the sensor array 4c to be stored and correlated with particular forms of input code from the optical fibre 2b.

The output from the sensor array 4 comprises an electrical signal 3a which is applied to the electrical conduit 2a.

A conventional digital processor 5a such as a Pentium ™ or similar digital processor with an associated input filter functionality 4a is coupled to the electrical conduit 2a. The filter functionality may provided by software running on the processor or by the provision of an individual processor dedicated to the filtering function. The processor 5a includes a conventional memory and holds a number of different algorithms/programs that can be used to decipher the encrypted code on the conduit 2a. In use, the processor 5a uses the algorithms to attempt to break the code. The processor 5a tries all of the individual programs in a sequence. As an example one of the algorithms may configured as described in "Breaking DES", Paul C Kocher, published by RASA Laboratories in CryptoBytes, the Technical newsletter of

RSA Laboratories, a Division of RSA Data Security Inc, Volume 4, Number 2, Winter 1999. Another algorithm may be as described in "Attacking Elliptic Curve Cryptosystems Using Parallel Pollard rho Method" by Adrian E Escott, Alexander P L Selkirk & Dimitrios Tsapakidis, in the same publication.

The incoming data from the conduit 2a is provided with an identification label by the processor 5a. This label is communicated through the backplane 2 to the other processors 5b, 5c where it is stored and associated with the filtered outputs produced by the filters 4b and 4c. This common label is used to associate the coded signal with the most efficient method employed to crack the code.

Once the processor 5a has identified a solution for the encrypted data, it carries out a sanity check on the solution and possibly refers the solution to a human operator for final checking, on output 6a. Then, assuming that the solution satisfies the criteria, the previously mentioned code label associated with the encrypted signals is associated with the solution itself. This association performs two functions. The first is to allow the machine to learn, so that each time a code is entered into the machine and has already been labelled, then the machine, from its previous experience knows what algorithms are suited to solving it. Thus, the processor 5ais directed to perform algorithmic processing in a particular sub-set of its possible range of possibilities rather than use the complete set of algorithms that are available, thereby speeding up the process.

The processor 5a also carries out a checking of the solution obtained from the code breaking algorithms in order to determine whether a solution has been found or whether further attempts to break the code are required using different algorithms.

An example will now be considered in which the machine shown in Figure 5 is used to crack a signature or password that was created by multiplying two prime numbers. The machine thus is required to determine the two prime numbers from encrypted data comprising the multiplication thereof on input I.

The problem of trying to crack the code with a conventional digital processor requires the processor to number crunch through each and every combination of prime numbers until an appropriate corresponding encrypted code is produced, so as to determine the solution. The speed at which the code will be cracked, is indeterminate as it is a function of where in the number of possibilities available, the algorithm started to check the various combinations.

When the machine of Figure 5 is first switched on, it has no knowledge of the characteristics of the encrypted signal applied to input I or which algorithm should be employed in processor 5a to crack the code. When the first encoded signal is presented to the machine, all of the processors 5a, b, c operate on the signal. As a first operation, the coded signal is characterised by each of the processors and associated with the aforementioned label generated by processor 5a. Once characterised, the machine is able to identify the form of the code, in this case the multiplication of two prime numbers. This may need intervention by a human operator. Having identified the make up of the code, the processor 5a will employ one of a number of number-crunching algorithms to crack the code. The first time that the machine carries out this process, it does not know where to start the algorithm and therefore the process may take along time. Once having cracked the code, the processor 5a will associate the code label with the corresponding solution so as to associate a particular part of the solution space provided by the algorithm with the solution. Each time a new code is presented to the machine, it will start to build a knowledge of the corresponding labels associated with the incoming data which relate to the code characteristics so as to learn where to look for a solution rather than try all possible solutions.

When the machine is initially turned on, instead of just applying a coded signal that requires decoding, it will be possible to take a range of codes which the user has created and therefore for which the solution is known, and use these to teach the machine.

Claims

1. Data processing apparatus comprising:
a backplane for data signals in a plurality of different formats,
a plurality of adaptive filters to receive data signals in respective different formats from the backplane, and
a plurality of processors to receive data derived from the backplane in said different formats respectively, at least one of the processors being operable to process data from one of the filters and being responsive to the outcome of data filtering performed by at least one other of the filters to adapt the processing performed thereby.

2. Apparatus according to claim 1 including a feedback path to adjust filtering characteristics of at least one of the adaptive filters as a function of the outcome of the processing performed by at least one of the processors.

3. Apparatus according to claim 1 or 2 wherein at least one of the processors is operable to carry out processing according to a plurality of different algorithms and to select at least one of them according to the outcome of processing performed by another of the processors.

4. Apparatus according to any preceding claim wherein the backplane includes an first conduit for signals in a first format and a second conduit for signals in a second format.

5. Apparatus according to claim 4 wherein the filters include a first filter to filter the signals in the first conduit and a second filter to filter the signals in the second conduit.

6. Apparatus according to claim 4 or 5 wherein the processors include a first processor to process signals derived from the first conduit and a second processor to process signals derived from the second conduit.

7. Apparatus according to claim 4, 5 or 6 including an input to receive input signals to be processed and to supply the signals to the first and second conduits in the first and second formats.

8. Apparatus according to any one of claims 4 to 7 wherein the first and second conduits are configured to convey optical and electrical signals respectively.

9. A data processing method for data manifested as signals in a plurality of different formats, comprising:
adaptively filtering the data signals in the different formats respectively, and individually processing the signals in said different formats respectively, such as to process data in one of the formats that has been subject to the adaptive filtering, adaptively in response to the outcome of data filtering performed on data in at least one other of the formats.

10. A method according to claim 9 including adjusting the filtering of data in one of the formats as a function of the outcome of the processing performed in another of the formats.

11. A method according to claim 9 or 10 including selecting the processing for data in one of the formats from a plurality of different algorithms according to the outcome of processing performed on the data in another of the formats.

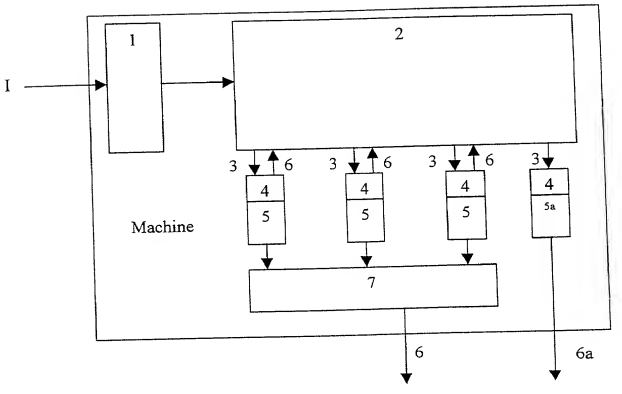

Fig. 1

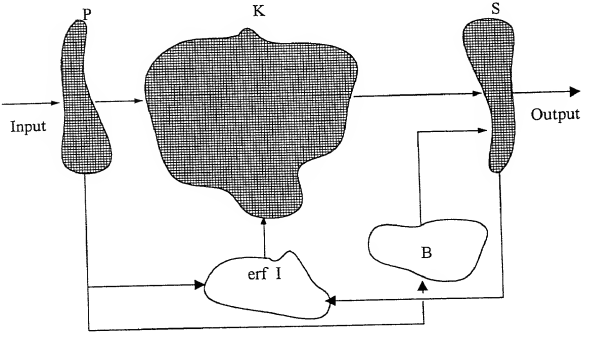

Fig. 2

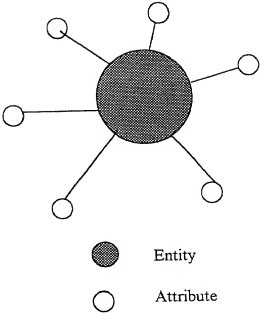

Fig. 3

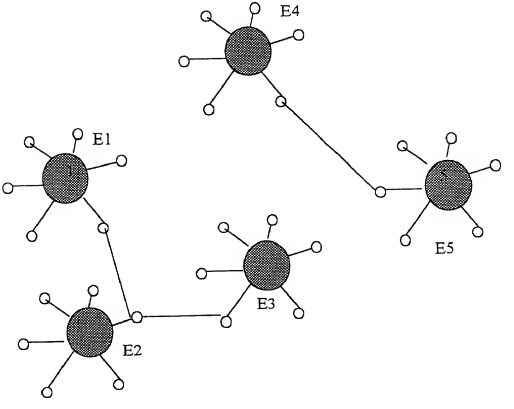

Fig. 4

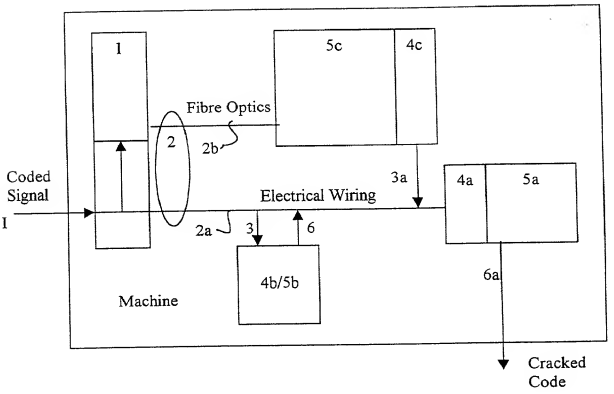
1
5c
4c
Fibre Optics
2
2b
Coded
Signal
I
3a
4a
5a
Electrical Wiring
2a
3
6
4b/5b
6a
Machine
Cracked
Code

Fig. 5

Nixon & Vanderhye P.C. (10/99)
(Domestic Non-Assigned/Foreign)

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DATA PROCESSING APPARATUS

the specification of which (**check** applicable **box(s)**):

☐ is attached hereto
☐ was filed on _____ as U.S. Application Serial No. _____ (Atty Dkt. No. _____)
☒ was filed as PCT international application No. PCT/GB00/02531 on 30 June 2000
and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
99305219.0	EUROPE	01 JULY 1999

☐ I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed

☐ I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): Application Serial No.	Day/Month/Year Filed	Status: patented pending, abandoned
PCT/GB00/02531	30 June 2000	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And on behalf of the owner(s) hereof, I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively owner's/owners' attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31382; Richard G. Besha, 22779; Mark E. Nusbaum, 32349; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr., 29366; Thomas E. Byrne, 32205; Mary J. Wilson, 32955; J. Scott Davidson, 33489; Alan M. Kagen, 36178; Robert A. Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331; Frank P. Presta, 19828; Joseph S. Presta, 35329] also authorize Nixon & Vanderhye to delete any attorney names/numbers no longer with the firm and to act and rely solely on instructions directly communicated from the person, assignee, attorney, firm, or other organization sending instructions to Nixon & Vanderhye on behalf of the owner(s).

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FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Nixon & Vanderhye P.C. (12/95)

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